1700 V SCALE-iDriver

Up to 8 A Single Channel IGBT/MOSFET Gate Driver Providing Basic Galvanic Isolation for 1700 V IGBT and MOSFET

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Product Highlights

Highly Integrated, Compact Footprint

- Split outputs providing up to 8 A peak drive current
- Integrated FluxLink™ technology providing galvanic isolation between primary-side and secondary-side
- Rail-to-rail stabilized output voltage
- Unipolar supply voltage for secondary-side
- Suitable for 1700 V IGBT and MOSFET switches
- Up to 75 kHz switching frequency
- Low propagation delay time 260 ns
- Propagation delay jitter ±5 ns
- -40 °C to 125 °C operating ambient temperature
- High common-mode transient immunity
- eSOP package with 9.5 mm creepage and clearance distances

Advanced Protection / Safety Features

- Undervoltage lock-out protection for primary and secondary-side (UVLO) and fault feedback
- Short-circuit protection using $V_{CE\ SAT}$ monitoring and fault feedback
- Advanced Soft Shut Down (ASSD)

Full Safety and Regulatory Compliance

- 100% production partial discharge test
- 100% production HIPOT compliance testing at 6 kV RMS 1 s
- Basic insulation meets VDE 0884-10

Green Package

- Halogen free and RoHS compliant

Applications

- General purpose and servo drives
- UPS, solar, welding inverters and power supplies

Description

The SID1183K is a single channel IGBT and MOSFET driver in an eSOP package. Galvanic isolation is provided by Power Integrations' innovative solid insulator FluxLink technology. The up to 8 A peak output drive current enables the product to drive devices up to 600 A without requiring any additional active components. For gate drive requirements that exceed the stand-alone capability of the SID1183K, an external booster may be added. Stable positive and negative voltages for gate control are provided by one unipolar isolated voltage source.

Additional features are short-circuit protection (DESAT) with Advanced Soft Shut Down (ASSD), undervoltage lock-out (UVLO) for primary-side and secondary-side and rail-to-rail output with temperature and process compensated output impedance guarantee safe operation even in harsh conditions.

Controller (PWM and fault) signals are compatible with 5 V CMOS logic, which may also be adjusted to 15 V levels by using external resistor divider.

Product Portfolio

Product[1]	Peak Output Drive Current
SID1183K	8 A

Table 1. SCALE-iDriver 1700 V Portfolio.
Notes:
1. Package: eSOP-R16B.

Figure 2. eSOP-R16B Package.

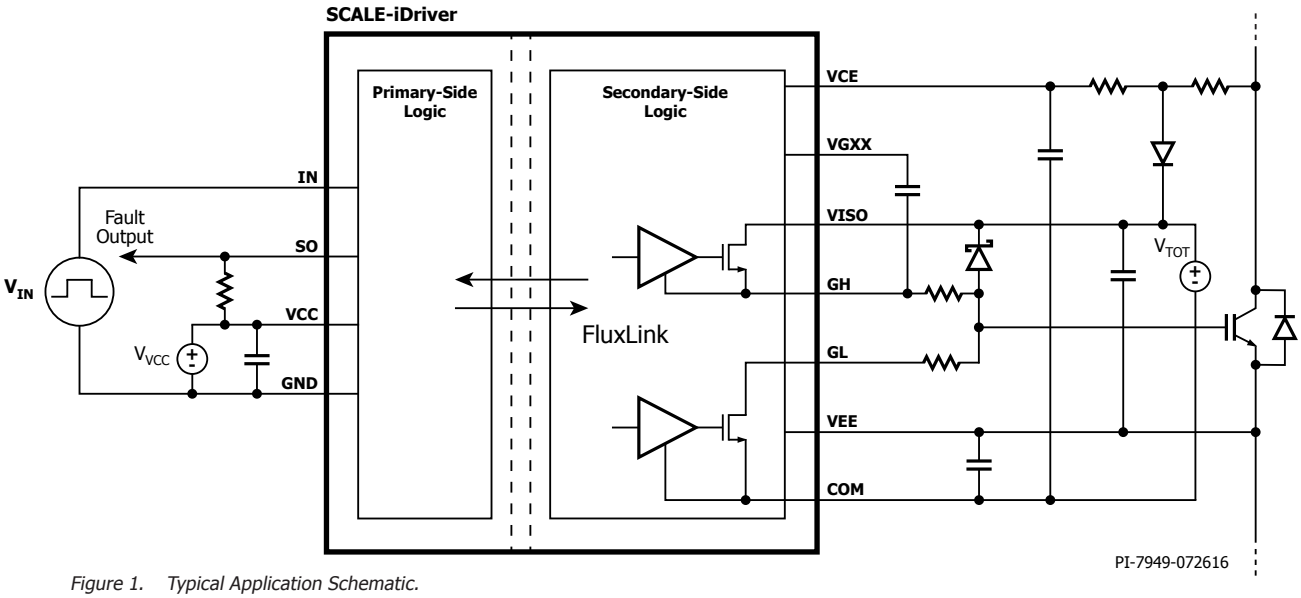


Figure 1. Typical Application Schematic.

This Product is Covered by Patents and/or Pending Patent Applications.

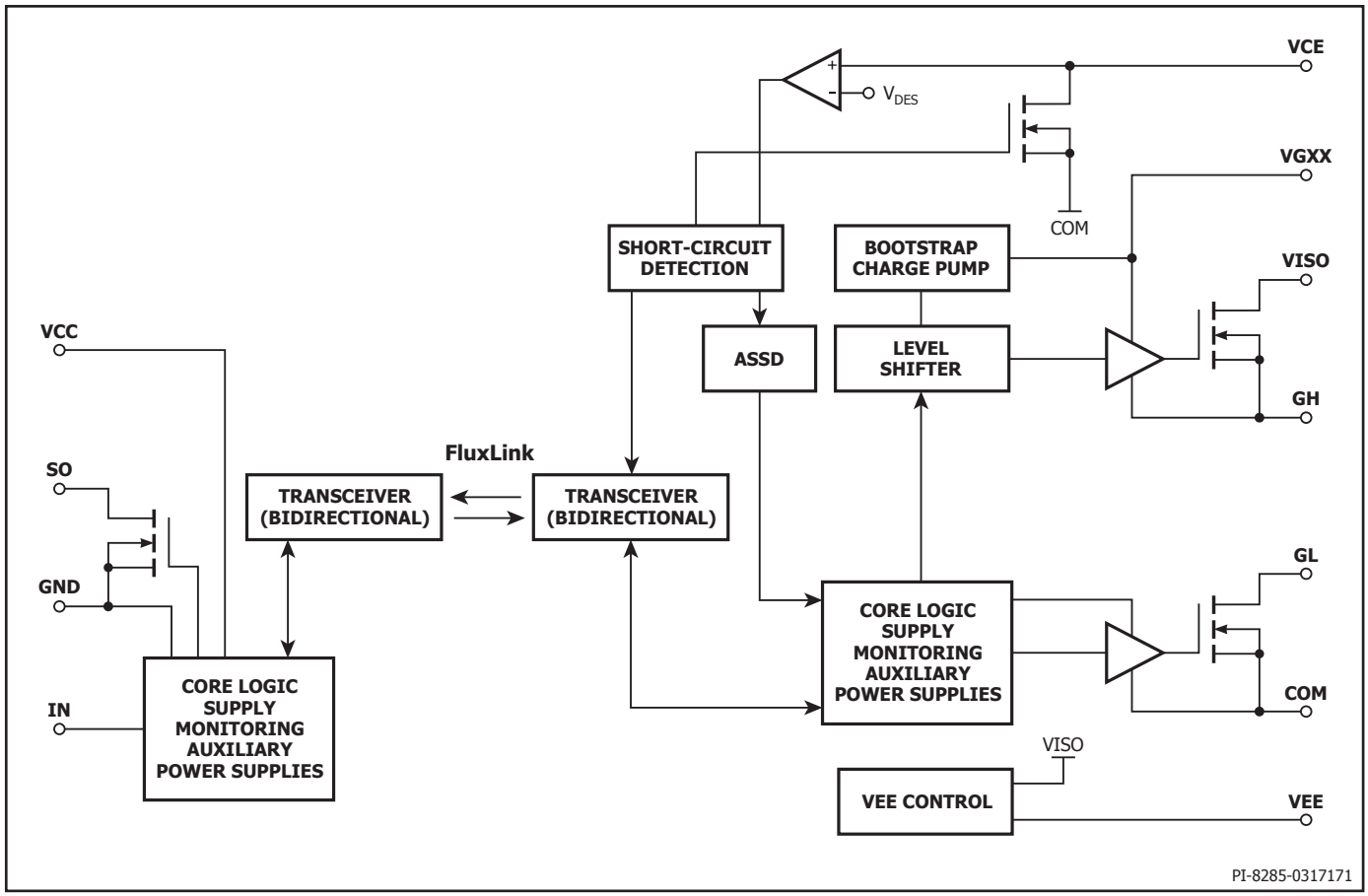


Figure 3. Functional Block Diagram.

Pin Functional Description

VCC Pin (Pin 1):
This pin is the primary-side supply voltage connection.

GND Pin (Pin 3-6):
This pin is the connection for the primary-side ground potential. All primary-side voltages refer to this pin.

IN Pin (Pin 7):
This pin is the input for the logic command signal.

SO Pin (Pin 8):
This pin is the output for the logic fault signal (open drain).

NC Pin (Pin 9):
This pin must be un-connected. Minimum PCB pad size for soldering is required.

VEE Pin (Pin 10):
Common (IGBT emitter/MOSFET source) output supply voltage.

VCE Pin (Pin 11):
This pin is the desaturation monitoring voltage input connection.

VGXX Pin (Pin 12):
This pin is the bootstrap and charge pump supply voltage source.

GH Pin (Pin 13):
This pin is the driver output – sourcing current (turn-on) connection.

VISO Pin (Pin 14):
This pin is the input for the secondary-side positive supply voltage.

COM Pin (Pin 15):
This pin provides the secondary-side reference potential.

GL Pin (Pin 16):
This pin is the driver output – sinking current (turn-off).

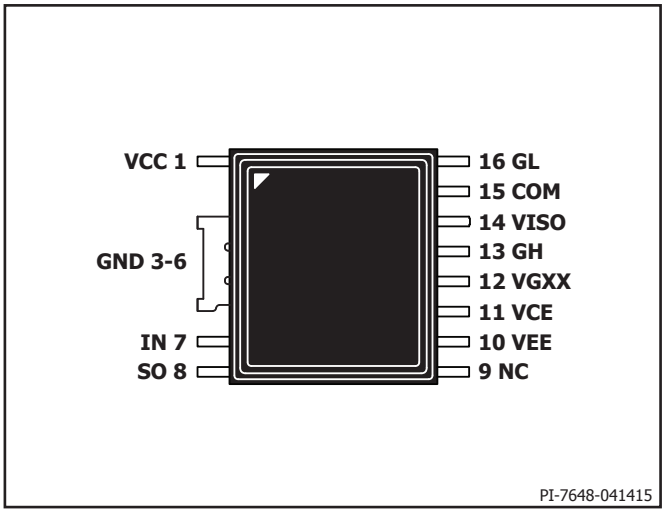


Figure 4. Pin Configuration.

SCALE-iDriver Functional Description

The single channel SCALE-iDriver™ family drives IGBTs and MOSFETs or other semiconductor power switches with a blocking voltage of up to 1700 V and provides basic isolation between micro-controller and the power semiconductor switch. The status of the power semiconductor switch and SCALE-iDriver is monitored via the SO pin.

Command signals are transferred from the primary (IN) to secondary-side via FluxLink isolation technology. The GH pin supplies a positive gate voltage and charges the semiconductor gate during the turn-on process. The GL pin supplies the negative voltage and discharges the gate during the turn-off process.

Short-circuit protection is implemented using a desaturation detection technique monitored via the VCE pin. After the SCALE-iDriver detects a short-circuit, the semiconductor turn-off process is implemented using an Advanced Soft Shut Down (ASSD) technique.

Power Supplies

The SID1183K requires two power supplies. One is the primary-side (V_{VCC}) which powers the primary-side logic and communication with the secondary (insulated) side. One supply voltage is required for the secondary-side, V_{TOT} is applied between the VISO pin and the COM pin. V_{TOT} should be insulated from the primary-side and should provide at least the same insulation capabilities as the SCALE-iDriver. V_{TOT} should have a low capacitive coupling to the primary or any other secondary-side. The positive gate-emitter voltage is provided by V_{VISO} which is internally generated and stabilized to 15 V (typically) with respect to VEE. The negative gate-emitter voltage is provided by V_{VEE} with respect to COM. Due to the limited current sourcing capabilities of the VEE pin, any additional load needs to be applied between the VISO and COM pins. No additional load between VISO and VEE pins or between VEE and COM pins is allowed.

Input and Fault Logic (Primary-Side)

The input (IN) and output (SO) logic is designed to work directly with micro-controllers using 5 V CMOS logic. If the physical distance between the controller and the SCALE-iDriver is large or if a different logic level is required, the resistive divider in Figure 5 is recommended. This solution adjusts the logic level as necessary and will also improve the driver's noise immunity.

Gate driver commands are transferred from the IN pin to the GH and GL pins with a propagation delay $t_{P(LH)}$ and $t_{P(HL)}$.

During normal operation, when there is no fault detected, the SO pin stays at high impedance (open). Any fault is reported by connecting the SO pin to GND. The SO pin stays low as long as the V_{VCC} voltage (primary-side) stays below $UVLO_{VCC}$, and the propagation delay is negligible. If desaturation is detected (there is a short-circuit), or the supply voltages V_{VISO}, V_{VEE}, (secondary-side) drop below $UVLO_{VISO}$, $UVLO_{VEE}$, the SO status changes with a delay time t_{FAULT} and keeps status low for a time defined as t_{SO}. In case of a fault condition the driver applies the off-state (the GL pin is connected to COM). During the t_{SO} period, command signal transitions from the IN pin are ignored. A new turn-on command transition is required before the driver will enter the on-state.

The SO pin current is defined as I_{SO}; voltage during low status is defined as $V_{SO(FAULT)}$.

Output (Secondary-Side)

The gate of the power semiconductor switch should be connected to the SCALE-iDriver output via pins GH and GL, using suitable turn-on and turn-off gate resistors. Turn-on gate resistor R_{GON} needs to be connected to the GH pin and turn-off gate resistor R_{GOFF} to the GL pin. If both gate resistors have the same value, the GL and GH pins may be connected together. Note: The SCALE-iDriver SID1183K data sheet defines the R_{GH} and R_{GL} values as total resistances connected to the respective pins GH and GL. Note that most power semiconductor data sheets specify an internal gate resistor R_{GINT} which is already integrated into the power semiconductor switch. In addition to R_{GINT}, external resistor devices R_{GON} and R_{GOFF} are specified to setup the gate current levels to the application requirements. Consequently, R_{GH} is the sum of R_{GON} and R_{GINT}, as shown in Figures 9 and 10. Careful consideration should be given to the power dissipation and peak current associated with the external gate resistors.

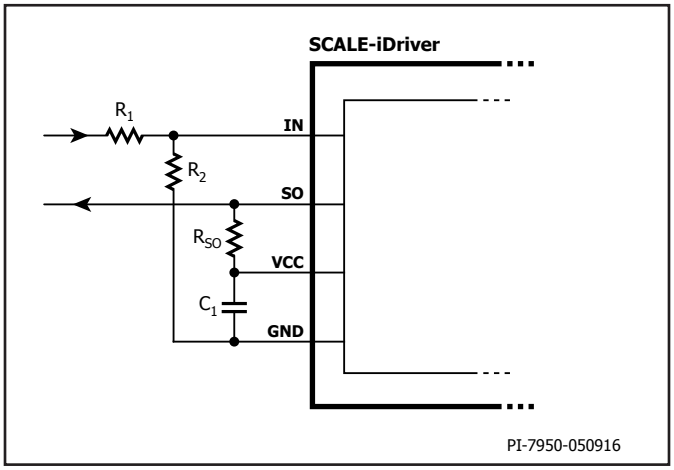


Figure 5. Increased Threshold Voltages V_{IN+LT} and V_{IN+HT}. For R_1 = 3.3 kΩ and R_2 = 1 kΩ the IN Logic Level is 15 V.

The GH pin output current source (I_{GH}) of SID1183K is capable of handling (typically) up to 7.3 A during turn-on, and the GL pin output current source (I_{GL}) is able to sink up to 8.0 A during turn-off at 25 °C. The SCALE-iDriver's internal resistances are described as R_{GHI} and R_{GLI} respectively. If the gate resistors for SCALE-iDriver family attempt to draw a higher peak current, the peak current will be internally limited to a safe value, see Figures 6 and 7. Figure 8 shows the peak current that can be achieved for a given supply voltage for same gate resistor values, load capacitance and layout design.

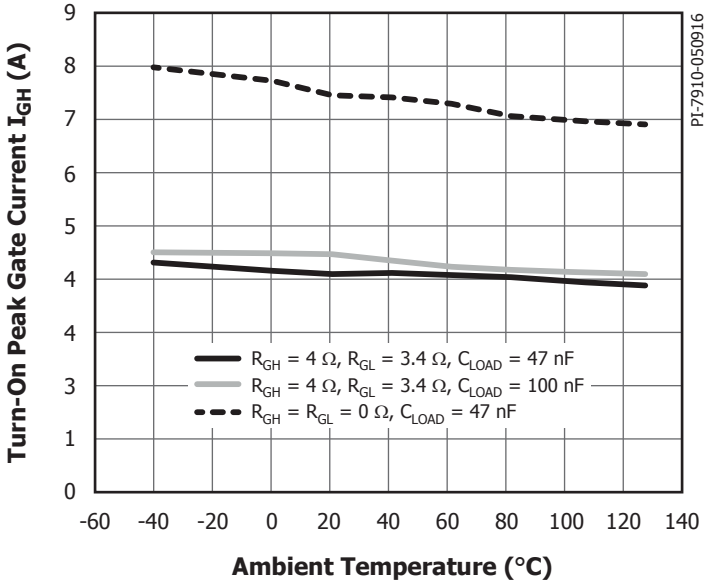


Figure 6. Turn-On Peak Output Current (Source) vs. Ambient Temperature. Conditions: V_{CC} = 5 V, V_{TOT} = 25 V, f_S = 20 kHz, Duty Cycle = 50%.

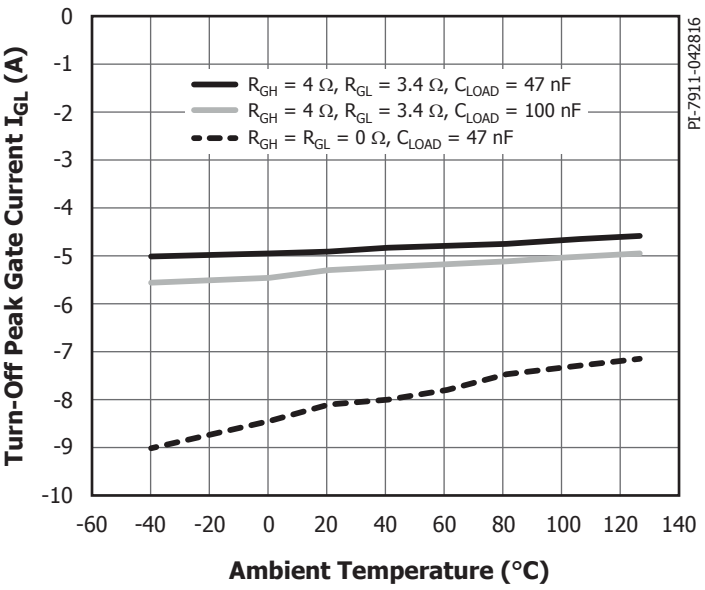


Figure 7. Turn-Off Peak Output Current (Sink) vs. Ambient Temperature. Conditions: V_{VCC} = 5 V, V_{TOT} = 25 V, f_S = 20 kHz, Duty Cycle = 50%.

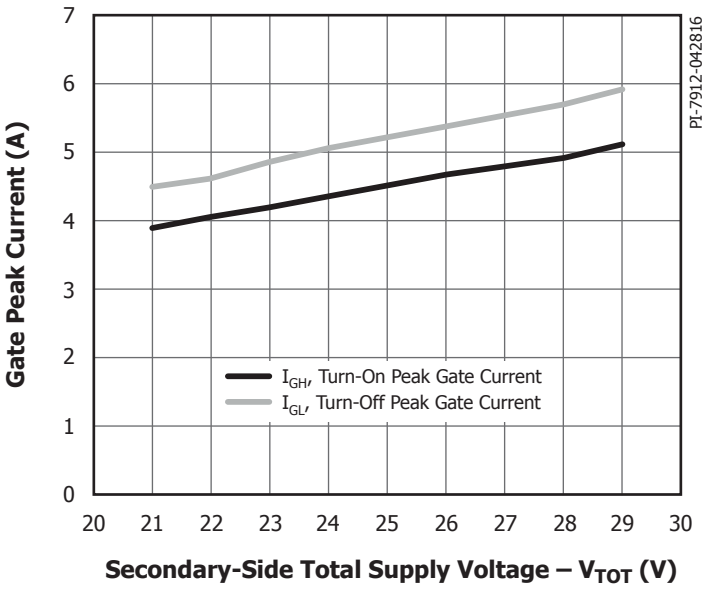


Figure 8. Turn-On and Turn-Off Peak Output Current vs. Secondary-Side Total Supply Voltage (V_{TOT}). Conditions: V_{VCC} = 5 V, T_J = 25 °C, R_{GH} = 4 Ω, R_{GL} = 3.4 Ω, C_{LOAD} = 100 nF, f_S = 1 kHz, Duty Cycle = 50%.

Short-Circuit Protection

The SCALE-iDriver uses the semiconductor desaturation effect to detect short-circuits and protects the device against damage by employing an Advanced Soft Shut Down (ASSD) technique. Desaturation can be detected using two different circuits, either with diode sense circuitry D_{VCE} (Figure 9) or with resistors R_{VCEX} (Figure 10). With the help of a well stabilized V_{VISO} and a Schottky diode (D_{STO}) connected between semiconductor gate and VISO pin the short-circuit current value can be limited to a safe value.

During the off-state, the VCE pin is internally connected to the COM pin and C_{RES} is discharged (red curve in Figure 11 represents the potential of the VCE pin). When the power semiconductor switch receives a turn-on command, the collector-emitter voltage (V_{CE}) decreases from the off-state level same as the DC-link voltage to a normally much lower on-state level (see blue curve in Figure 11) and C_{RES} begins to be charged up to the V_{CE} saturation level ($V_{CE\ SAT}$). The V_{CE} voltage during on-state is continuously observed and compared with a reference voltage V_{DES}. As soon as V_{CE}>V_{DES} the driver turns off the power semiconductor switch with a controlled collector current slope, limiting the V_{CE} overvoltage excursions to below the maximum collector-emitter voltage (V_{CES}). Turn-on commands during this time and during t_{SO} are ignored, and the SO pin is connected to GND.

The response time t_{RES} is the C_{RES} charging time and describes the delay between V_{CE} asserting and the voltage on the VCE pin rising (see Figure 11). Response time should be long enough to avoid false tripping during semiconductor turn-on and is adjustable via R_{RES} and C_{RES} (Figure 9) or R_{VCE} and C_{RES} (Figure 10) values. It should not be longer than the period allowed by the semiconductor manufacturer.

Note: The response time for short-circuit protection using a resistor network depends also on the actual DC-link voltage.

The implementation according to Figure 10 is preferred as it avoids unintended tripping of the gate driver during zero-crossing of the load current, which depending on actual application conditions may lead to a transient V_{CESAT} increase. The circuitry according to Figure 10 provides an inherent filter, which prevents a false short-circuit detection. The implementation according to Figure 9, however, does not provide this filtering and may lead to unintended tripping events.

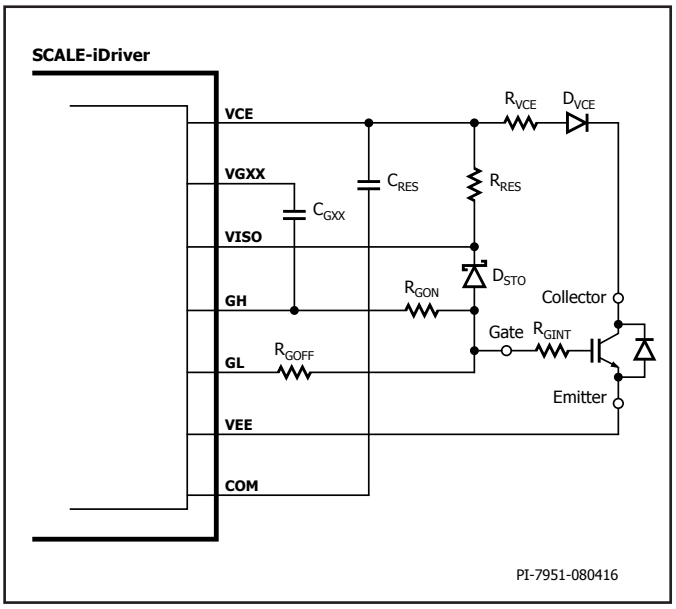


Figure 9. Short-Circuit Protection Using Diode D_{VCE}.

Safe Power-Up and Power-Down

During power-up and power-down the IN pin should stay at logic low. In order to avoid these effects, it is recommended that the IN pin is kept at logic low during power-up and power-down. Any supply voltage related to VCC, VISO, VEE and VGXX pins should be stabilized using ceramic capacitors C_1, C_{S1X}, C_{S2X}, C_{GXX} respectively as shown in Figures 13 and 14. After supply voltages reach their nominal values, the driver will begin to function after a time delay t_{START}.

Short-Pulse Operation

If command signals applied to the IN pin are shorter than the minimum specified by $t_{GE(MIN)}$, then SID1183K output signals, GH and GL pins, will extend to value $t_{GE(MIN)}$. The duration of pulses longer than $t_{GE(MIN)}$ will not be changed.

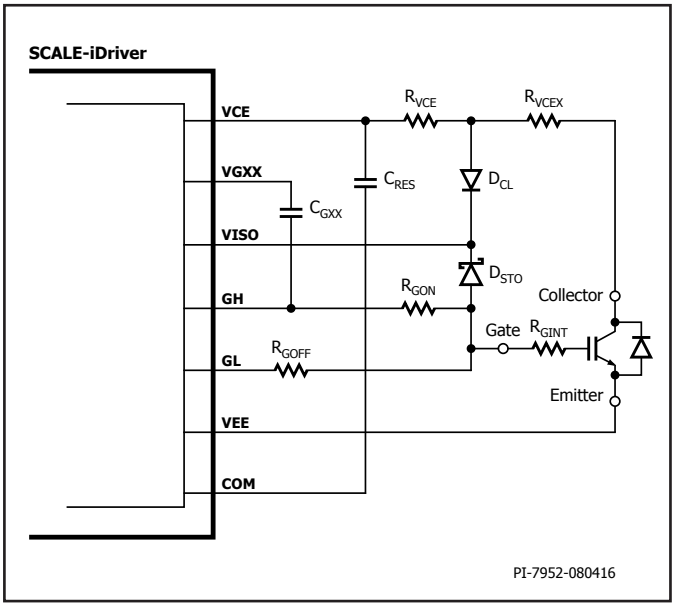


Figure 10. Short-Circuit Protection Using a Resistor Network R_{VCEX}.

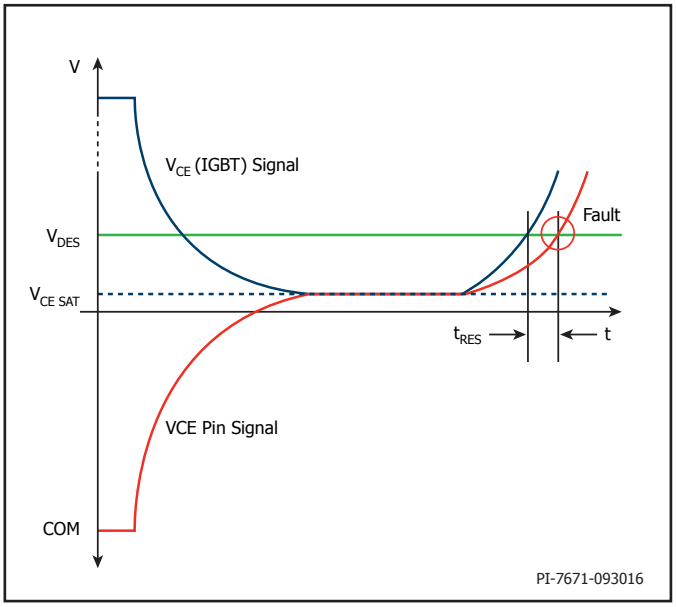


Figure 11. Short-Circuit Protection Using Resistor Network R_{VCEX}.

Advanced Soft Shut Down (ASSD)

This function is activated after a short-circuit is detected. It protects the power semiconductor switch against destruction by ending the turn-on state and limiting the current slope in order to keep momentary V_{CE} overvoltages below V_{CES}. This function is particularly suited to IGBT applications. Figure 12 shows how the ASSD function operates. The V_{CE} desaturation is visible during time period P1 (yellow line). During this time, the gate-emitter voltage (green line) is kept very stable. Collector current (pink line) is also well stabilized and limited to a safe value. At the end of period P1, V_{GE} is reduced until the beginning of t_{FSSD1}. Due to collector current decrease a small V_{CE} overvoltage is seen. During t_{FSSD1} V_{GE} is further reduced and the gate of the power semiconductor switch is further discharged. During t_{FSSD2} additional small V_{CE} overvoltage events may occur. Once V_{GE} drops below the gate threshold of the IGBT, the collector current has decayed almost to zero and the remaining gate charge is removed – ending the short- circuit event. The whole short-circuit current detection and safe switch-off is shorter than 10 µs (7.1 µs from 10%-to-10% of the collector current in this example).

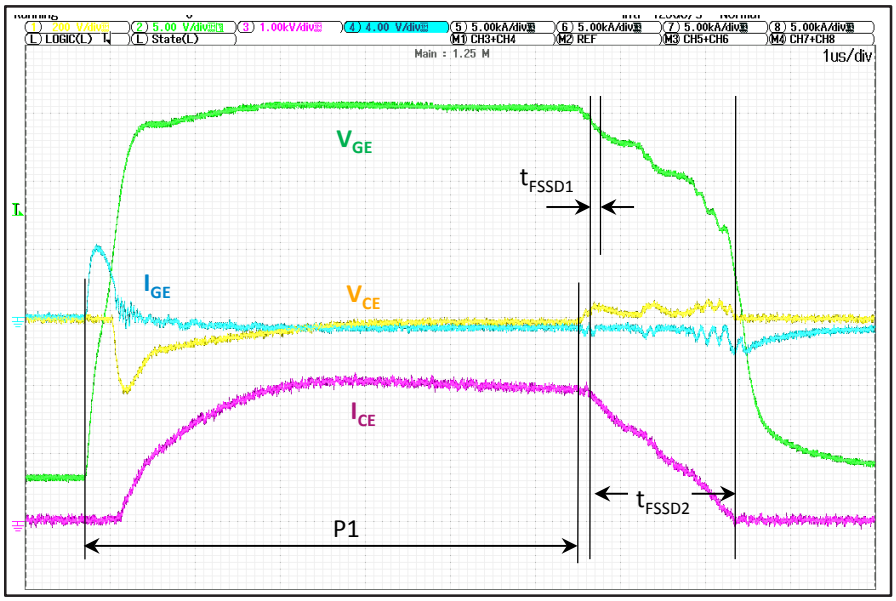


Figure 12. Advanced Soft Shut Down Function.

Application Examples and Components Selection

Figures 13 and 14 show the schematic and typical components used for a SID1183K design. In both cases the primary-side supply voltage (V_{VCC}) is connected between VCC and GND pins and supported through a supply bypass ceramic capacitor C_1 (4.7 µF typically). If the command signal voltage level is higher than the rated IN pin voltage (in this case 15 V) a resistive voltage divider should be used. Additional capacitor C_F and Schmitt trigger IC_1 can be used to provide input signal filtering. The SO output has 5 V logic and the R_{SO} is selected so that it does not exceed absolute maximum rated I_{SO} current.

The secondary-side isolated power supply (V_{TOT}) is connected between VISO and COM. The positive voltage rail (V_{VISO}) is supported through 4.7 µF ceramic capacitors C_{S21} and C_{S22} connected in parallel. The negative voltage rail (V_{VEE}) is similarly supported through capacitors C_{S11} and C_{S12}. The gate charge will vary according to the type of power semiconductor switch that is being driven. Typically, $C_{S11} + C_{S12}$ should be at least 3 µF multiplied by the total gate charge of the power semiconductor switch (Q_{GATE}) divided by 1 µC. A 10 nF capacitor C_{GXX} is connected between the GH and VGXX pins.

The gate of the power semiconductor switch is connected through resistor R_{GON} to the GH pin and by R_{GOFF} to the GL pin. If the value of R_{GON} is the same as R_{GOFF} the GH pin can be connected to the GL pin and a common gate resistor can be connected to the gate. In each case, proper consideration needs to be given to the power dissipation and temperature performance of the gate resistors.

To ensure gate voltage stabilization and collector current limitation during a short-circuit, the gate is connected to the VISO pin through a Schottky diode D_{STO} (for example PMEG4010).

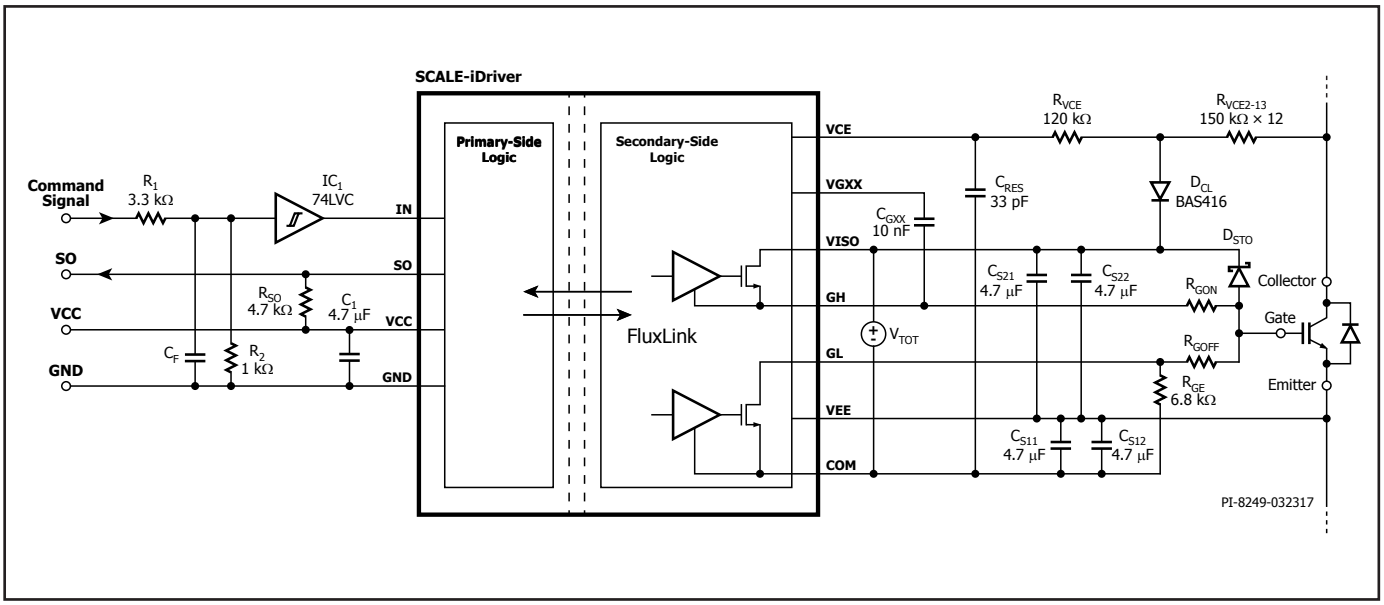


Figure 13. SCALE-iDriver Application Example Using a Resistor Network for Desaturation Detection.

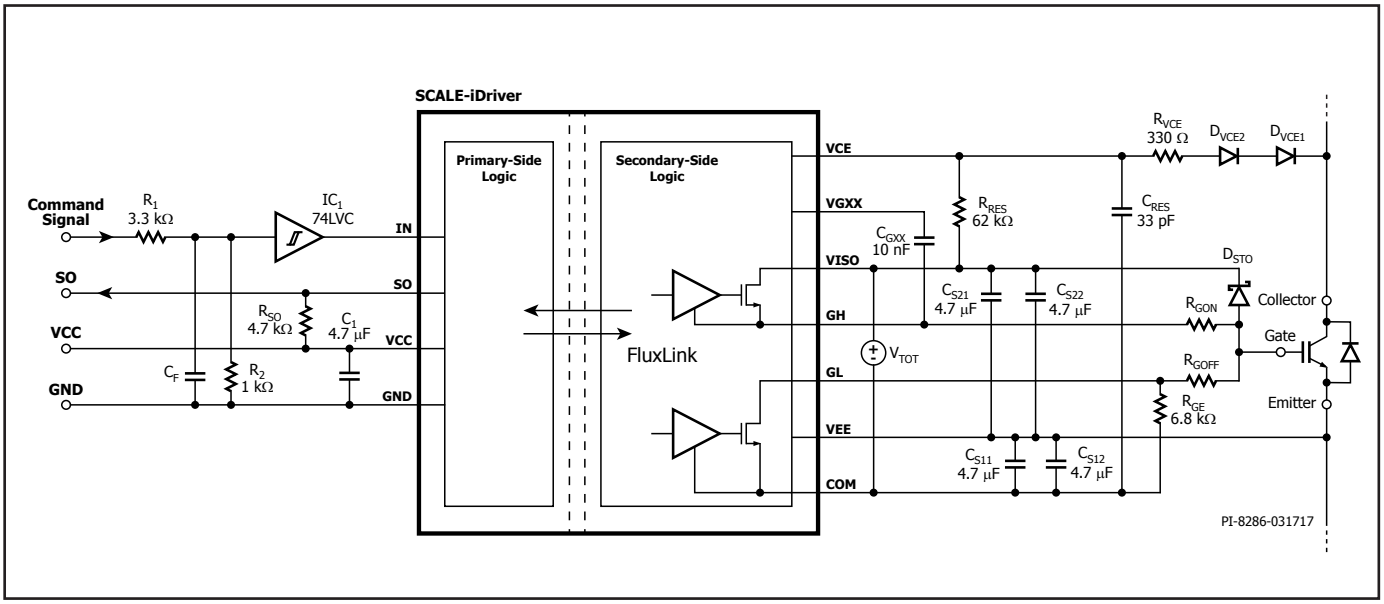


Figure 14. SCALE-iDriver Application Example Using Diodes for Desaturation Detection.

To avoid parasitic power-switch-conduction during system power-on, the gate is connected to COM through 6.8 kΩ resistor.

Figure 13 shows how switch desaturation can be measured using resistors R_{VCE2} – R_{VCE13}. In this example all the resistors have a value of 150 kΩ and 1206 size. The total resistance is 1.8 MΩ. The resistors should be chosen to limit current to between 0.6 mA to 0.8 mA at maximum DC-link voltage. The sum of R_{VCE2} – R_{VCE13} should be typically 1.8 MΩ for 1700 V semiconductors. In each case the resistor string must provide sufficient creepage and clearance distances between collector of the semiconductor and SCALE-iDriver. The low leakage diode D_{CL} keeps the short-circuit duration constant over a wide DC-link voltage range.

Response time is set up through R_{VCE} and C_{RES} (typically 120 kΩ and 33 pF respectively for 1700 V semiconductors). If short-circuit detection proves to be too sensitive, the C_{RES} value can be increased. The maximum short-circuit duration must be limited to the maximum value given in the semiconductor data sheet.

Figure 14 illustrates how diodes D_{VCE1} and D_{VCE2} may be used to measure switch desaturation. For insulation, two or more diodes in SMD packages are used (STTH212U for example depending on actual application conditions). R_{RES} connected to VISO guarantees current flow through the diodes when the semiconductor is in the on-state. When the switch desaturates, C_{RES} starts to be charged through R_{RES}. In this configuration the response time is controlled by R_{RES} and C_{RES}. In this application example C_{RES} = 33 pF and R_{RES} = 62 kΩ; if desaturation is too sensitive or the short-circuit duration too long, both C_{RES} and R_{RES} can be adjusted.

Figure 15 shows the recommended PCB layout and corresponds to the schematic in Figure 13. The PCB is a two layer design. It is important to ensure that PCB traces do not cover the area below the desaturation resistors or diodes D_{VCE1} and D_{VCE2}. This is a critical design requirement to avoid coupling capacitance with the SCALE-iDriver's VCE pin and isolation issues within the PCB.

Gate resistors are located physically close to the power semiconductor switch. As these components can get hot, it is recommended that they are placed away from the SCALE-iDriver.

Power Dissipation and IC Junction Temperature Estimation

First calculation in designing the power semiconductor switch gate driver stage is to calculate the required gate power - P_{DRV}. The power is calculated based on equation 1:

$$P_{DRV} = Q_{GATE} \times f_S \times V_{TOT} \quad (1)$$

where,

Q_{GATE} – Controlled power semiconductor switch gate charge (derived for the particular gate potential range defined by V_{TOT}). See semiconductor manufacturer data sheet.

f_S – Switching frequency which is same as applied to the IN pin of SCALE-iDriver.

V_{TOT} – SCALE-iDriver secondary-side supply voltage.

In addition to P_{DRV}, P_P (primary-side IC power dissipation) and P_{SNL} (secondary-side IC power dissipation without capacitive load) must be considered. Both are ambient temperature and switching frequency dependent (see typical performance characteristics).

$$P_P = V_{VCC} \times I_{VCC} \quad (2)$$
$$P_{SNL} = V_{TOT} \times I_{VISO} \quad (3)$$

During IC operation, the P_{DRV} power is shared between turn-on (R_{GH}), turn-off (R_{GL}) external gate resistors and internal driver resistances R_{GHI} and R_{GLI}. For junction temperature estimation purposes, the dissipated power under load (P_{OL}) inside the IC can be calculated accordingly to equation 4:

$$P_{OL} = 0.5 \times Q_{GATE} \times f_S \times V_{TOT} \times \left(\frac{R_{GHI}}{R_{GHI} + R_{GH}} + \frac{R_{GLI}}{R_{GLI} + R_{GL}} \right) \quad (4)$$

R_{GH} and R_{GL} represent sum of external (R_{GON}, R_{GOFF}) and power semiconductor internal gate resistance (R_{GINT}):

$$R_{GH} = R_{GON} + R_{GINT}$$
$$R_{GL} = R_{GOFF} + R_{GINT}$$

Total IC power dissipation (P_{DIS}) is estimated as sum of equations 2, 3 and 4:

$$P_{DIS} = P_P + P_{SNL} + P_{OL} \quad (5)$$

The operating junction temperature (T_J) for given ambient temperature (T_A) can be estimated according to equation 6:

$$T_J = \theta_{JA} \times P_{DIS} + T_A \quad (6)$$

Example

An example is given below,

f_S = 20 kHz, T_A = 85 °C, V_{TOT} = 25 V, V_{VCC} = 5 V.
Q_{GATE} = 1.5 μC (the gate charge value here should correspond to selected V_{TOT}), R_{GINT} = 2.5 Ω, R_{GON} = R_{GOFF} = 1.8 Ω.

P_{DRV} = 1.5 μC × 20 kHz × 25 V = 0.75 W, according to equation 1.
P_P = 5 V × 13.5 mA = 68 mW, according to equation 2 (see Figure 18).
P_{SNL} = 25 V × 7.7 mA = 193 mW, according to equation 3 (see Figure 20).

The dissipated power under load is:

$$\mathrm{P_{OL}} = 0.5 \times 1.5\,\mu\mathrm{C} \times 20\ \mathrm{kHz} \times 25\ \mathrm{V} \times \left(\frac{1.2\ \Omega}{1.2\ \Omega + 4.3\ \Omega} + \frac{1.1\ \Omega}{1.1\ \Omega + 4.3\ \Omega} \right) \cong 176\ mW,$$

according to equation 4.

R_{GHI} = 1.2 Ω as maximum data sheet value.
R_{GLI} = 1.1 Ω as maximum data sheet value.
R_{GH} = R_{GL} = 1.8 Ω + 2.5 Ω = 4.3 Ω.

P_{DIS} = 68 mW + 193 mW + 176 mW = 437 mW according to equation 5.
T_J = 67 °C/W × 437 mW + 85 °C = 113 °C according to equation 6.

Estimated junction temperature for this design would be approximately 113 °C and is lower than the recommended maximum value. As the internal IC resistor values are maximum values, it is understood that the example represents worst-case conditions.

Table 2 describes the recommended capacitor and resistor characteristics and layout requirements to achieve optimum performances of SCALE-iDriver.

Pin	Return to Pin	Recommended Value	Symbol	Notes
VCC	GND	4.7 µF	C_1	VCC blocking capacitor must be placed close to IC. Enlarged loop could result in inadequate VCC supply voltage during operation.
VISO	VEE	4.7 µF	C_{S21}/C_{S22}	25V X7R type is recommended. Example part number could be Murata 25 V part #GRM31CR71E475KA88. This capacitor needs to be close to IC pins.
VEE	COM	4.7 µF	C_{S11}/C_{S12}	25 V X7R type is recommended. Example part number could be Murata 25 V part #GRM31CR71E-475KA88. This capacitor needs to be close to IC pins.
VGXX	GH	10 nF	C_{GXX}	To avoid misoperation, this pin should not be connected to anything else. This capacitor needs to be as close to IC pins as possible. 25 V X7R type is recommended. Example part number could be Yageo 25 V part#CC0603KRX7R9BB103.
VCE	COM	33 pF	C_{RES}	Select C_{RES} to achieve needed desaturation protection response time. 50 V COG/NPO is recommended. A value of 33 pF is initially recommended. Example part number could be KEMET 50 V part C0603C330J5GACTU. Any net and any other layer should provide sufficient distance to components C_{RES} in order to avoid parasitic effects (capacitance)
VCE			R_{VCE}, D_{VCE}, C_{RES}, R_{RES}, D_{CL}	Select R_{VCE} or R_{RES} for the proper operation of the short-circuit protection. Any net and any other layer should provide sufficient distance to components R_{VCE}, D_{VCE}, R_{RES}, and D_{CL} in order to avoid parasitic effects.

Table 2. PCB Layout and Component Guidelines.

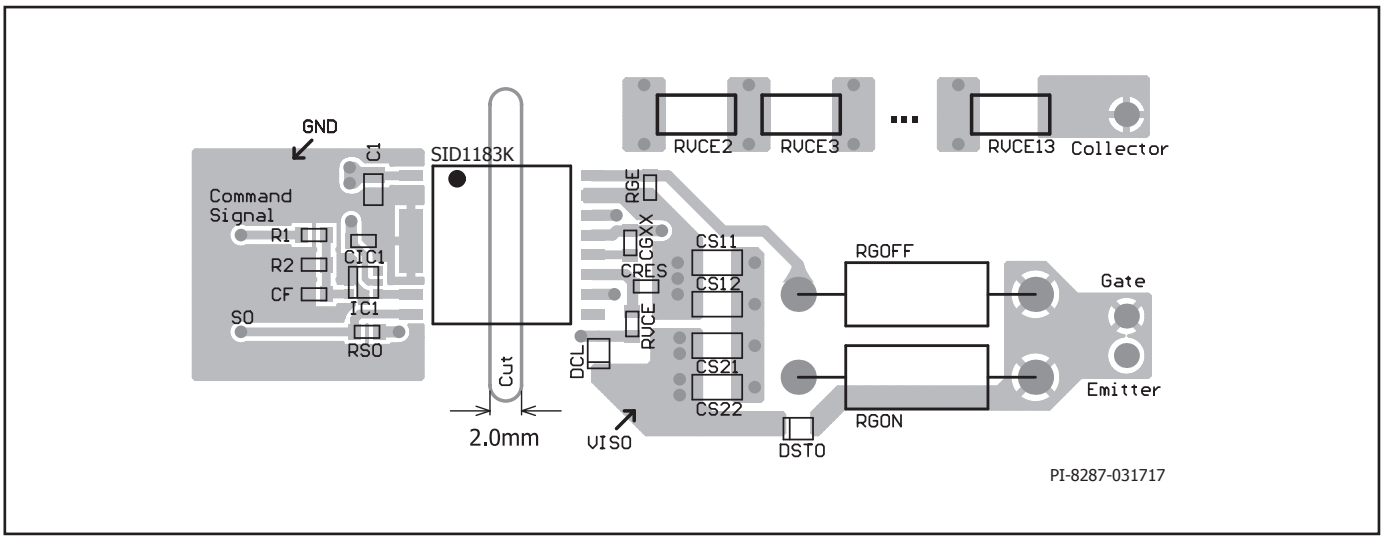


Figure 15a. Top View of Recommended PCB Layout. Corresponds to Schematic Shown in Figure 13.

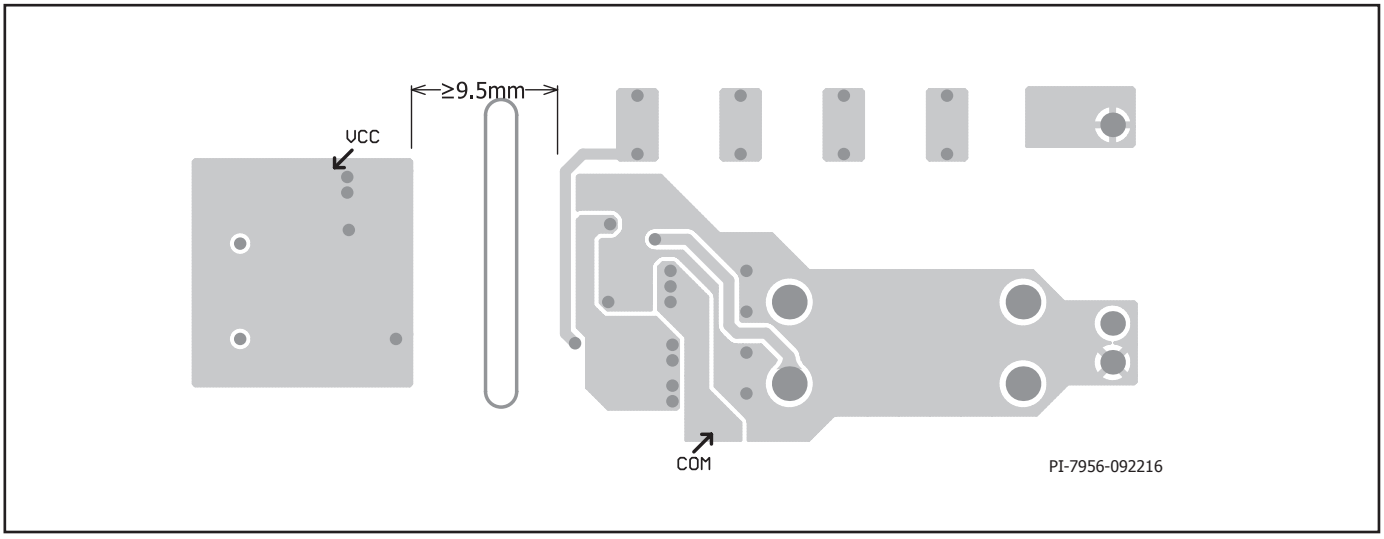


Figure 15b. Bottom View of Recommended PCB Layout. Corresponds to Schematic Shown in Figure 13.

Parameter	Symbol	Conditions	Min	Max	Units
Absolute Maximum Ratings[1]					
Primary-Side Supply Voltage[2]	V_{VCC}	VCC to GND	-0.5	6.5	V
Secondary-Side Total Supply Voltage	V_{TOT}	VISO to COM	-0.5	30	V
Secondary-Side Positive Supply Voltage	V_{VISO}	VISO to VEE	-0.5	17.5	V
Secondary-Side Negative Supply Voltage	V_{VEE}	VEE to COM	-0.5	15	V
Logic Input Voltage (command signal)	V_{IN}	IN to GND	-0.5	V_{VCC} + 0.5	V
Logic Output Voltage (fault signal)	V_{SO}	SO to GND	-0.5	V_{VCC} + 0.5	V
Logic Output Current (fault signal)	I_{SO}	Positive Current Flowing into the Pin		10	mA
VCE Pin Voltage	V_{VCE}	VCE - COM	-0.5	V_{TOT} + 0.5	V
Switching Frequency	f_S			75	kHz
Storage Temperature	T_S		-65	150	°C
Operating Junction Temperature	T_J		-40	150[3]	°C
Operating Ambient Temperature	T_A		-40	125	°C
Operating Case Temperature	T_C		-40	125	°C
Input Power Dissipation[4]	P_P	V_{VCC} = 5 V V_{TOT} = 28 V		115	mW
Output Power Dissipation[4]	P_S			1675	
Total IC Power Dissipation[4]	P_{DIS}			1790	mW

NOTES:

1. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.
2. Defined as peak voltage measured directly on VCC pin.
3. Transmission of command signals could be affected by PCB layout parasitic inductances at junction temperatures higher than recommended.
4. Input Power Dissipation refers to equation 2. Output Power Dissipation is secondary-side IC power dissipation without capacitive load (P_{SNL}, equation 3) and dissipated power under load (P_{OL}, equation 4). Total IC power dissipation is sum of P_P and P_S.

Thermal Resistance

Thermal Resistance: eSOP-R16B Package:

θ_{JA} ..... 67 °C/W[1]

θ_{JC} ..... 34 °C/W[2]

Notes:

1. 2 oz. (610 g/m^2) copper clad. Measured with layout shown in Figure 15.
2. The case temperature is measured at the plastic surface at the top of the package.

Parameter	Symbol	Conditions T_J = -40 °C to +125 °C See Note 1 (Unless Otherwise Specified)	Min	Typ	Max	Units
Recommended Operation Conditions						
Primary-Side Supply Voltage	V_{VCC}	VCC - GND	4.75		5.25	V
Secondary-Side Total Supply Voltage	V_{TOT}	VISO - COM	22		28	V
Logic Low Input Voltage	V_{IL}				0.5	V
Logic High Input Voltage	V_{IH}		3.3			V
Switching Frequency	f_S		0		75	kHz
Operating IC Junction Temperature	T_J		-40		125	°C
Electrical Characteristics						
Logic Low Input Threshold Voltage	V_{IN+LT}	f_S = 0 Hz	0.6	1.25	1.8	V
Logic High Input Threshold Voltage	V_{IN+HT}	f_S = 0 Hz	1.7	2.2	3.05	V
Logic Input Voltage Hysteresis	V_{IN+HS}	f_S = 0 Hz	0.1			V
Input Bias Current	I_{IN}	V_{IN} = 5 V	56	113	165	µA
		V_{IN} > 3 V See Note 12		106		
Supply Current (Primary-Side)	I_{VCC}	V_{IN} = 0 V			17	mA
		V_{IN} = 5 V			23	
		f_S = 20 kHz			20	
		f_S = 75 kHz			23	
Supply Current (Secondary-Side)	I_{VISO}	V_{IN} = 0 V			8	mA
		V_{IN} = 5 V			9	
		f_S = 20 kHz			10	
		f_S = 75 kHz			14	
Power Supply Monitoring Threshold (Primary-Side)	$UVLO_{VCC}$	Clear Fault		4.28	4.65	V
		Set Fault	3.85	4.12		
		Hysteresis, See Notes 3, 4	0.02			
Power Supply Monitoring Threshold (Secondary-Side, Positive Rail V_{VISO})	$UVLO_{VISO}$	Clear Fault		12.85	13.5	V
		Set Fault, Note 3	11.7	12.35		
		Hysteresis	0.3			
Power Supply Monitoring Blanking Time, V_{VISO}	$UVLO_{VISO(BL)}$	Voltage Drop 13.5 V to 11.5 V See Note 12	0.5			µs
Power Supply Monitoring Threshold (Secondary-Side, Negative Rail V_{VEE})	$UVLO_{VEE}$	Clear Fault, V_{TOT} = 20 V		5.15	5.5	V
		Set Fault, V_{TOT} = 20 V	4.67	4.93		
		Hysteresis	0.1			

Parameter	Symbol	Conditions T_J = -40 °C to +125 °C See Note 1 (Unless Otherwise Specified)	Min	Typ	Max	Units
Electrical Characteristics (cont.)						
Power Supply Monitoring Blanking Time, V_{VEE}	$UVLO_{VEE(BL)}$	Voltage Drop 5.5 V to 4.5 V See Note 12	0.5			µs
Secondary-Side Positive Supply Voltage Regulation	$V_{VISO(HS)}$	21 V ≤ V_{TOT} ≤ 30 V, |i(VEE)| ≤ 1.5 mA	14.4	15.07	15.75	V
VEE Source Capability	$I_{VEE(SO)}$	V_{TOT} = 15 V, V_{VEE} set to 0 V	0.1			mA
		V_{TOT} = 25 V, V_{VEE} set to 7.5 V See Note 13	1.85	3.3	4.5	
VEE Sink Capability	$I_{VEE(SI)}$	V_{TOT} = 25 V, V_{VEE} set to 12.5 V	1.74	3.1	4.5	mA
DESAT Detection Level	V_{DES}	VCE-VEE, V_{IN} = 5 V	7.2	7.8	8.3	V
DESAT Sink Current	I_{DES}	V_{VCE} = 10 V, V_{IN} = 0 V	15	28	50	mA
DESAT Bias Current	$I_{DES(BS)}$	V_{VCE} - V_{VEE} = 4.5 V, V_{IN} = 5 V	-0.5		3	µA
VCE Pin Capacitance	C_{VCE}	Between VCE and COM pins See Note 12		12.5		pF
Turn-On Propagation Delay	$t_{P(LH)}$	T_J = 25 °C See Note 5	180	253	340	ns
		T_J = 125 °C See Note 5	210	278	364	
Turn-Off Propagation Delay	$t_{P(HL)}$	T_J = 25 °C See Note 6	200	262	330	ns
		T_J = 125 °C See Note 6	211	287	359	
Minimum Turn-On and Off Pulses	$t_{GE(MIN)}$	See Note 12			650	ns
Output Rise Time	t_R	No C_G See Note 7		22	45	ns
		C_G = 10 nF, See Note 7	55	90	150	
		C_G = 47 nF, See Note 7	300	465	650	
Output Fall Time	t_F	No C_G See Note 8		18	45	ns
		C_G = 10 nF See Note 8	40	81	150	
		C_G = 47 nF See Note 8	300	460	650	

Parameter	Symbol	Conditions T_J = -40 °C to +125 °C See Note 1 (Unless Otherwise Specified)	Min	Typ	Max	Units
Electrical Characteristics (cont.)						
ASSD Rate of Change	t_{FSSD1}	VGE change from 14.5 V to 14 V See Note 12		60		ns
	t_{FSSD2}	VGE change from 14.5 V to 2.5 V See Note 12	950	1828	2800	
Propagation Delay Jitter		See Note 12		±5		ns
Fault Signalization Delay Time	t_{FAULT}	See Note 10		190	750	ns
SO Fault Signalization time	t_{SO}		6.8	10	13.4	µs
Power-On Start-Up Time	t_{START}	See Note 11			10	ms
Gate Sourcing Peak Current, GH Pin	I_{GH}	$V_{GH} \geq V_{TOT}$ - 8.8 V C_G = 470 nF See Note 13	3.6	4.6	5.5	A
		R_G = 0, C_G = 47 nF See Notes 2, 12, 13 T_A = 25 °C		7.3		
Gate Sinking Peak Current GL Pin	I_{GL}	$V_{GL} \leq$ 7.5 V C_G = 470 nF V_{GL} is referenced to COM	4	4.8	5.5	A
		R_G = 0, C_G = 47 nF See Notes 2, 12 T_A = 25 °C		7.8		
Turn-On Internal Gate Resistance	R_{GHI}	I(GH) = 250 mA V_{IN}= 5 V See Note 13		0.76	1.2	Ω
Turn-Off Internal Gate Resistance	R_{GLI}	I(GL) = 250 mA V_{IN} = 0 V See Note 13		0.68	1.1	Ω
Turn-On Gate Output Voltage	$V_{GH(ON)}$	I(GH) = 20 mA V_{IN} = 5 V See Note 13	V_{TOT}-0.04			V

Parameter	Symbol	Conditions T_J = -40 °C to +125 °C See Note 1 (Unless Otherwise Specified)	Min	Typ	Max	Units
Electrical Characteristics (cont.)						
Turn-Off Gate Output Voltage (Referred to COM Pin)	$V_{GL(OFF)}$	I(GL) = 20 mA V_{IN} = 0 V			0.04	V
SO Output Voltage	$V_{SO(FAULT)}$	Fault Condition, I_{SO} = 3.4 mA, $V_{VCC} \geq$ 3.9 V		210	450	mV
Package Characteristics (See Notes 12, 14)						
Distance Through the Insulation	DTI	Minimum Internal Gap (Internal Clearance)	0.4			mm
Minimum Air Gap (Clearance)	L1 (IO1)	Shortest Terminal-to-Terminal Distance Through Air	9.5			mm
Minimum External Tracking (Creepage)	L2 (IO2)	Shortest Terminal-to-Terminal Distance Across the Package Surface	9.5			mm
Tracking Resistance (Comparative Tracking Index)	CTI	DIN EN 60112 (VDE 0303-11): 2010-05 EN / IEC 60112:2003 + A1:2009	600			
Isolation Resistance, Input to Output See Note 16	R_{IO}	V_{IO} = 500 V, T_J = 25 °C	10^{12}			Ω
		V_{IO} = 500 V, 100 °C ≤ T_J ≤ $T_{C(MAX)}$	10^{11}			
Isolation Capacitance, Input to Output See Note 16	C_{IO}			1		pF
Package Insulation Characteristics						
Maximum Working Isolation Voltage	V_{IOWM}				1202	V_{RMS}
Maximum Repetitive Peak Isolation Voltage	V_{IORM}				1700	V_{PEAK}
Input to Output Test Voltage	V_{PD}	Method A, After Environmental Tests Subgroup 1, V_{PR} = 1.3 × V_{IORM}, t = 10 s (qualification) Partial Discharge < 5 pC			2210	V_{PEAK}
		Method A, After Input/Output Safety Test Subgroup 2/3, V_{PR} = 1.2 x V_{IORM}, t = 10 s, (qualification) Partial Discharge < 5 pC			2040	
		Method B1, 100% Production Test, V_{PR} = 1.5 × V_{IORM}, t = 1 s Partial Discharge < 5 pC			2550	
Maximum Transient Isolation Voltage	V_{IOTM}	V_{TEST} = V_{IOTM}, t = 60 s (qualification), t = 1 s (100% production)			8000	V_{PEAK}
Maximum Surge Isolation Voltage	V_{IOSM}	Test Method Per IEC 60065, 1.2/50 µs Waveform, V_{TEST} = 1.3 x V_{IOSM} = 10400 V (qualification)			8000	V_{PEAK}
Insulation Resistance	R_S	V_{IO} = 500 V at T_S			>10^9	Ω
Maximum Case Temperature	T_S				150	°C

Parameter	Symbol	Conditions T_J = -40 °C to +125 °C See Note 1 (Unless Otherwise Specified)	Min	Typ	Max	Units
Package Insulation Characteristics (cont.)						
Safety Total Dissipated Power	P_S	T_J = 25 °C			1.79	W
Pollution Degree				2		
Climatic Classification				50/105/21		
Withstanding Isolation Voltage	V_{ISO}	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO} = 6000\ V_{RMS}$, t = 1 s (100% production)		5000		V_{RMS}

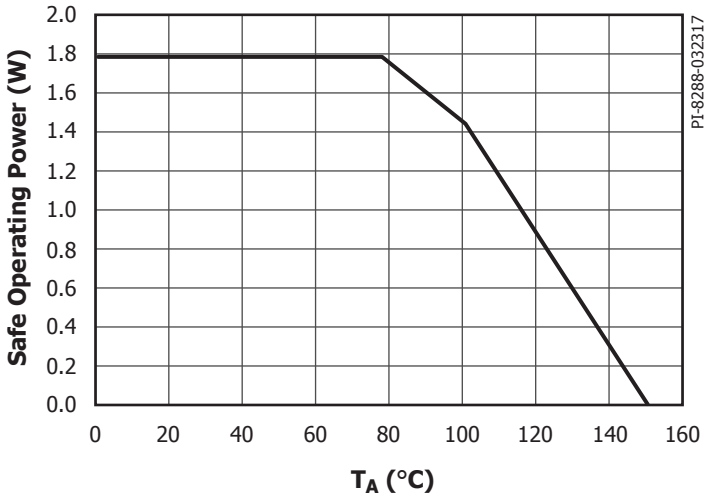


Figure 16. Thermal Derating Curve Showing Dependence of Limited Dissipated Power on Case Temperature (DIN V VDE V 0884-10).

Operation is allowed until reaching T_J and/or case temperature of 125 °C are reached. Thermal stress beyond those values but below thermal derating curve may lead to permanent functional product damage. Operating beyond thermal SR derating curve may affect product reliability.

NOTES:

1. V_{VCC} = 5 V, V_{TOT} = 25 V; GH and GL pins are shorted together. R_G = 4 Ω, No C_G; VCC pin is connected to the SO pin through a 2 kΩ resistor. The VGXX pin is connected to the GH pin through a 10 nF capacitor. Typical values are defined at T_J = 25 °C; f_S = 20 kHz, Duty Cycle = 50%. Positive currents are assumed to be flowing into pins.
2. Pulse width ≤ 10 μs, duty cycle ≤ 1%. The maximum value is controlled by the ASIC to a safe level. The internal peak power is safely controlled for $R_G \geq 0$ and power semiconductor module input gate capacitance C_{IES} ≤ 47 nF.
3. During very slow V_{VCC} power-up and power-down related to V_{TOT}, V_{VCC} and V_{VEE} respectively, several SO fault pulses may be generated.
4. SO pin connected to GND as long as V_{VCC} stays below minimum value. No signal is transferred from primary to secondary-side.
5. V_{IN} potential changes from 0 V to 5 V within 10 ns. Delay is measured from 50% voltage increase on IN pin to 10% voltage increase on GH pin.
6. V_{IN} potential changes from 5 V to 0 V within 10 ns. Delay is measured from 50% voltage decrease on IN pin to 10% voltage decrease on GL pin.
7. Measured from 10% to 90% of V_{GE} (C_G simulates semiconductor gate capacitance). The V_{GE} is measured across C_G.
8. Measured from 90% to 10% of V_{GE} (C_G simulates semiconductor gate capacitance). The V_{GE} is measured across C_G.
9. ASSD function limits G-E voltage of controlled semiconductor in specified time. Conditions: C_G = 10 nF, V_{TOT} = V_{VISO} = 15 V, V_{VEE} = 0 V (VEE shorted to COM).
10. The amount of time needed to transfer fault event (UVLO or DESAT) from secondary-side to SO pin.
11. The amount of time after primary and secondary-side supply voltages (V_{VCC} and V_{TOT}) reach minimal required level for driver proper operation. No signal is transferred from primary to secondary-side during that time, and no fault condition will be transferred from the secondary-side to the primary-side.
12. Guaranteed by design.
13. Positive current is flowing out of the pin.
14. Safety distances are application dependent and the creepage and clearance requirements should follow specific equipment isolation standards of an application. Board design should ensure that the soldering pads of an IC maintain required safety relevant distances.
15. Measured accordingly to IEC 61000-4-8 (f_S = 50 Hz, and 60 Hz) and IEC 61000-4-9.
16. All pins on each side of the barrier tied together creating a two-terminal device.

Typical Performance Characteristics

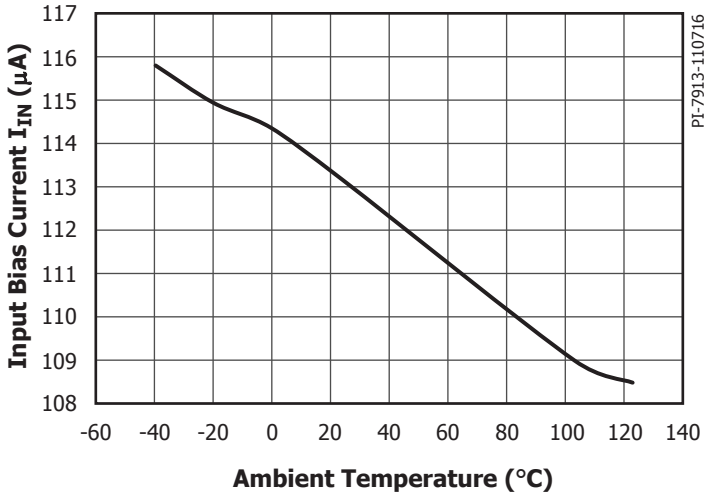


Figure 17. Input Bias Current vs. Ambient Temperature.
Conditions: V_{VCC} = 5 V, V_{IN} = 5 V, V_{TOT} = 25 V.

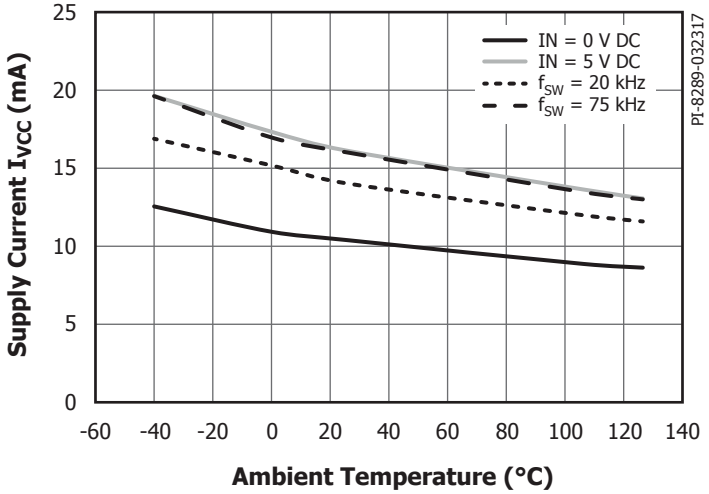


Figure 18. Supply Current Primary-Side I_{VCC} vs. Ambient Temperature.
Conditions: V_{VCC} = 5 V, V_{TOT} = 25 V, No-Load.

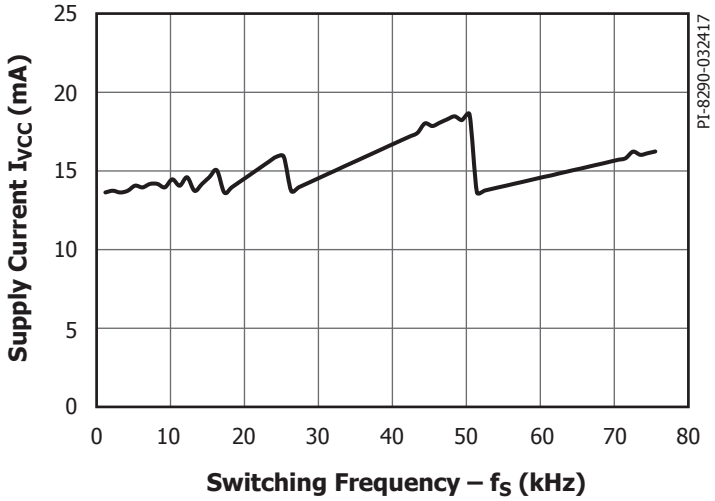


Figure 19. Supply Current Primary-Side I_{VCC} vs. Switching Frequency.
Conditions: V_{VCC} = 5 V, V_{TOT} = 25 V, T_J= 25 °C, No-Load.

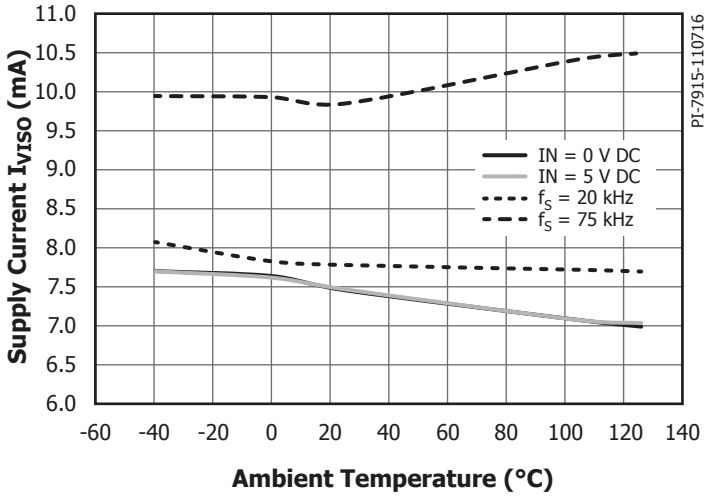


Figure 20. Supply Current Secondary-Side I_{VISO} vs. Ambient Temperature.
Conditions: V_{VCC} = 5 V, V_{TOT} = 25 V, No-Load.

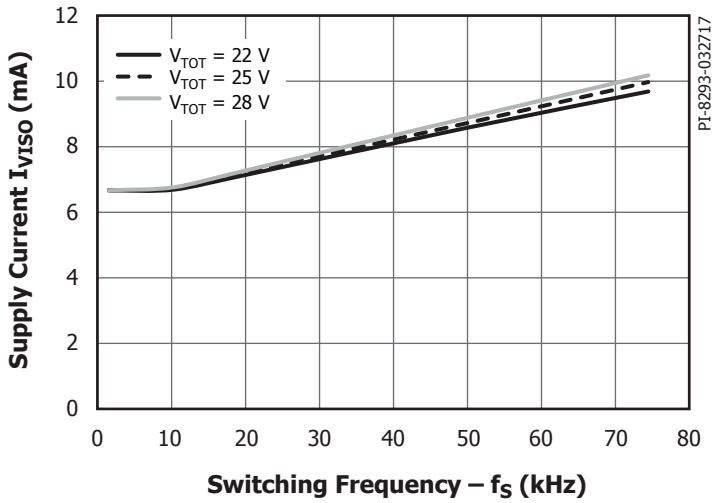


Figure 21. Supply Current Secondary-Side I_{VISO} vs. Switching Frequency.
Conditions: V_{VCC} = 5 V, No-Load.

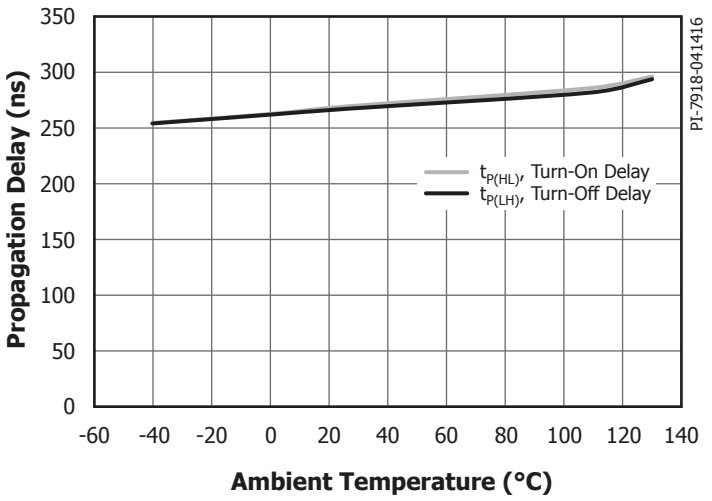


Figure 22. Propagation Delay Time vs. Ambient Temperature.
Conditions: V_{VCC} = 5 V, V_{TOT} = 25 V, f_S = 20 kHz, C_{LOAD} = 2.2 nF.

Typical Performance Characteristics

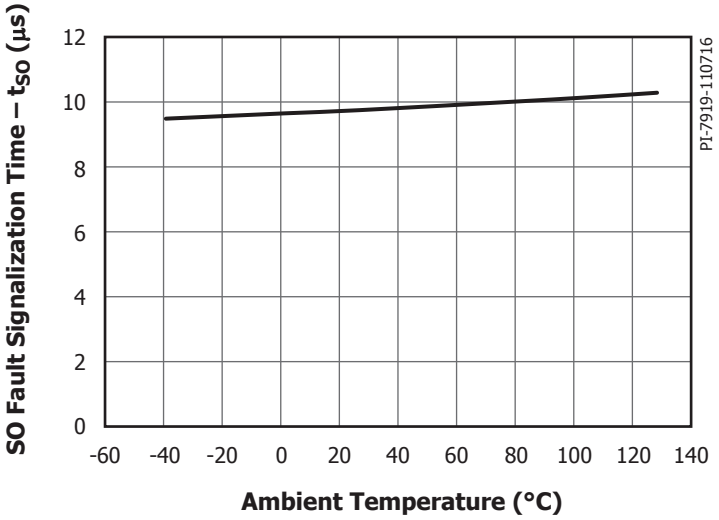


Figure 23. SO Fault Signalization Time vs. Ambient Temperature. Conditions: V_{VCC} = 5 V, V_{TOT} = 25 V, R_{SO} = 4.7 kΩ.

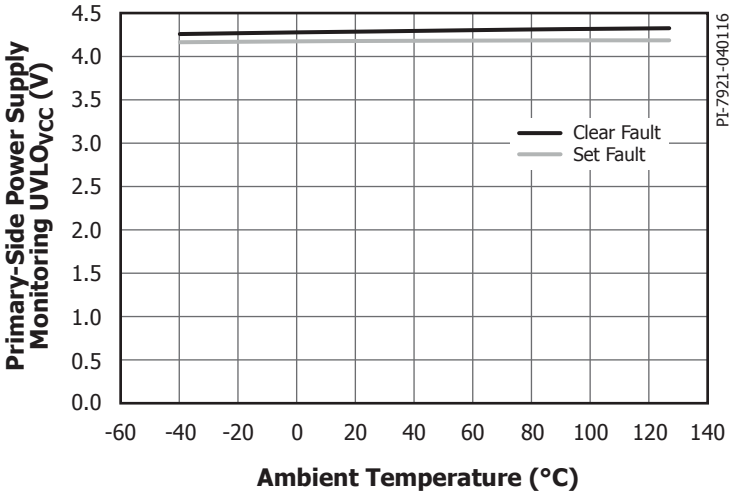


Figure 24. Power Supply Monitoring $UVLO_{VCC}$ vs. Ambient Temperature. Conditions: V_{TOT} = 25 V.

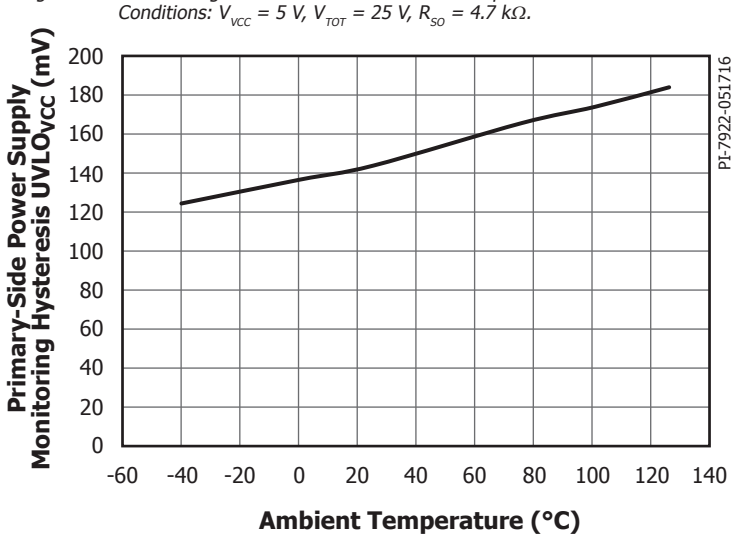


Figure 25. Power Supply Monitoring Hysteresis $UVLO_{VCC}$ vs. Ambient Temperature. Conditions: V_{TOT} = 25 V.

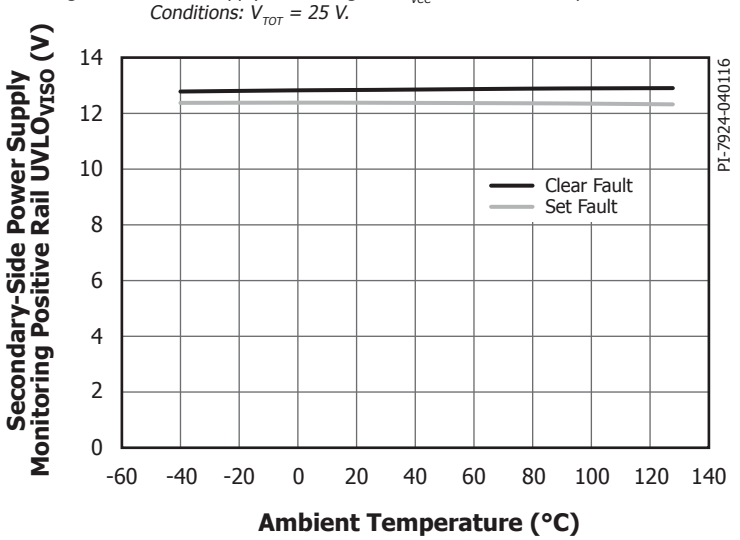


Figure 26. Power Supply Monitoring Positive Rail $UVLO_{VISO}$ vs. Ambient Temperature. Conditions: V_{VCC} = 5 V.

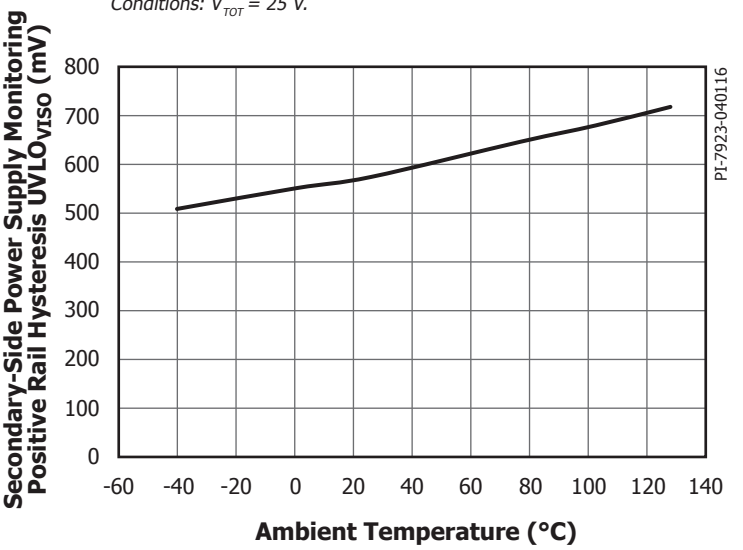


Figure 27 Power Supply Monitoring Positive Rail Hysteresis $UVLO_{VISO}$ vs. Ambient Temperature. Conditions: V_{VCC} = 5 V.

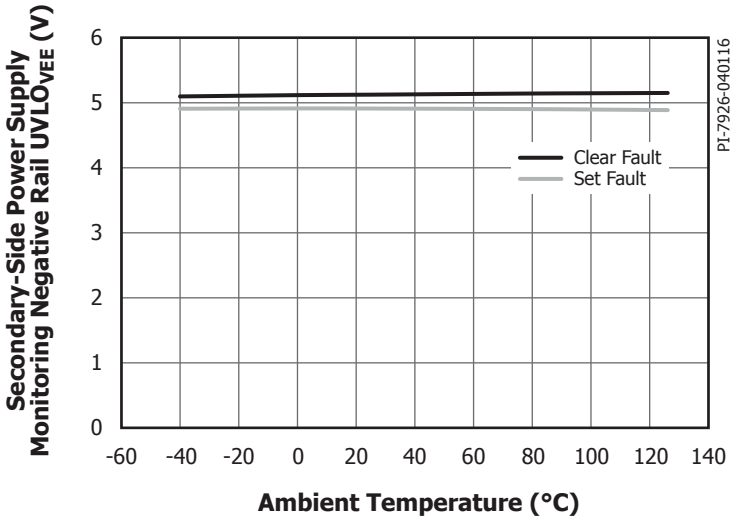


Figure 28. Power Supply Monitoring Negative Rail $UVLO_{VEE}$ vs. Ambient Temperature. Conditions: V_{VCC} = 5 V.

Typical Performance Characteristics

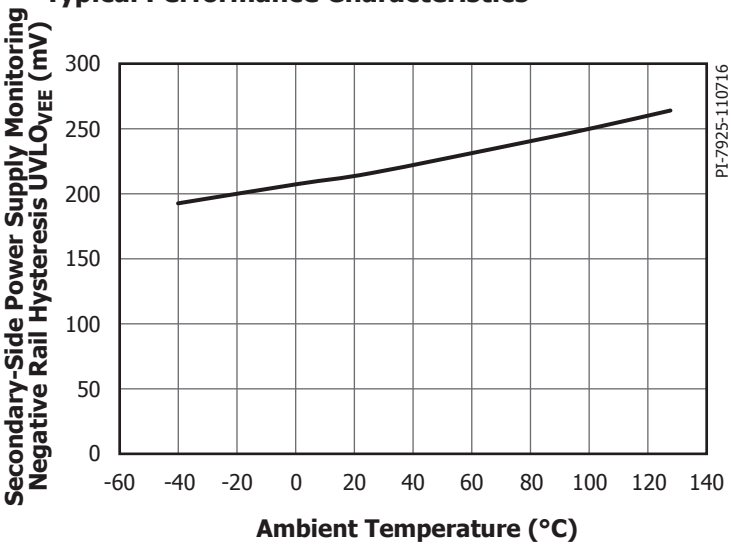


Figure 29. Power Supply Monitoring Negative Rail Hysteresis $UVLO_{VEE}$ vs. Ambient Temperature. Conditions: V_{VCC} = 5 V.

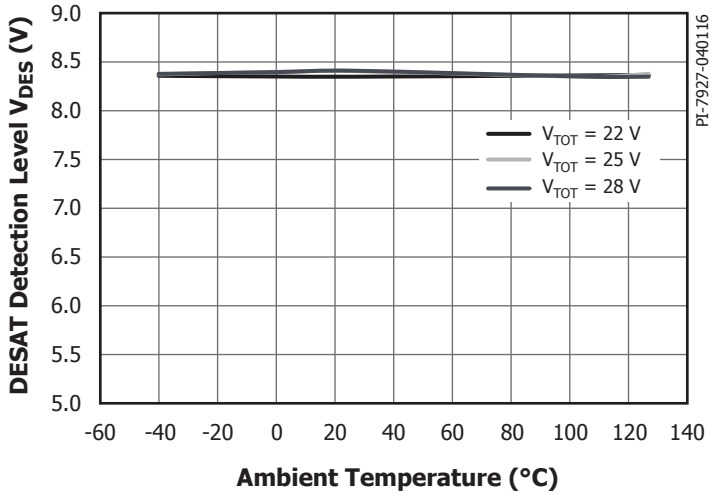


Figure 30. Desaturation Detection Level V_{DES} vs. Ambient Temperature. Conditions: V_{VCC} = 5 V.

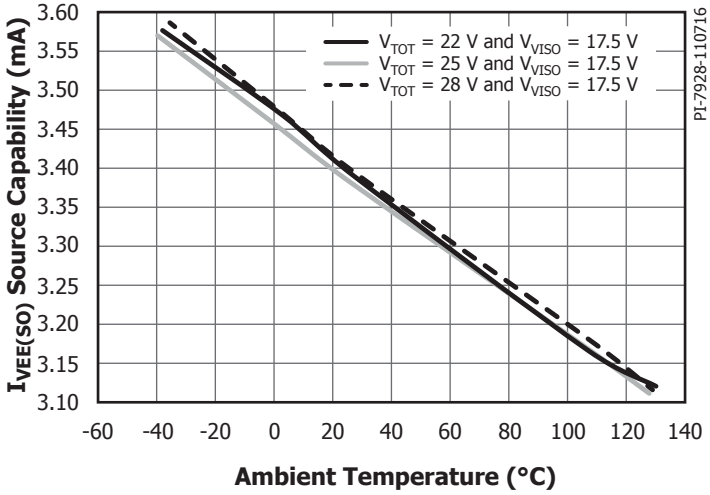


Figure 31. VEE Source Capability $I_{VEE(SO)}$ vs. Ambient Temperature and V_{VISO}. Conditions: V_{VCC} = 5 V, f_S = 20 kHz, Duty Cycle = 50%.

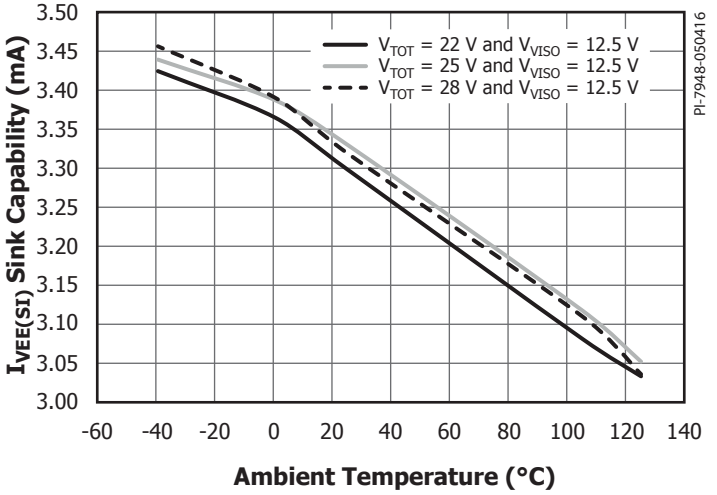
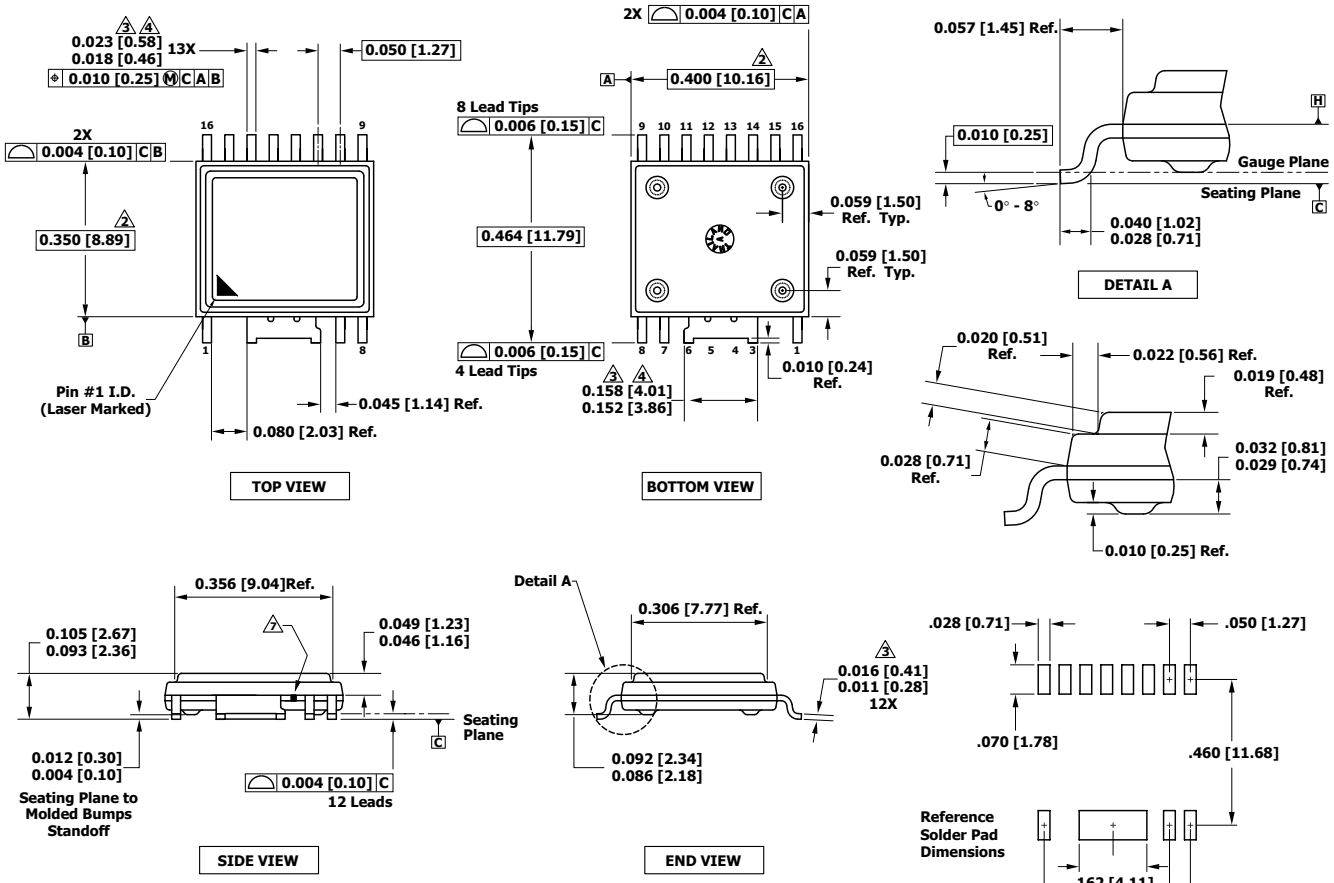


Figure 32. VEE Sink Capability $I_{VEE(SI)}$ vs. Ambient Temperature and V_{VISO}. Conditions: V_{VCC} = 5 V, f_S = 20 kHz, Duty Cycle = 50%.

eSOP-R16B



Notes:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and inter-lead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in inches [mm].
6. Datums A and B to be determined in Datum H.
7. Exposed metal at the plastic package body outline/surface between leads 6 and 7, connected internally to wide lead 3/4/5/6.

PI-6995-051716
POD-eSOP-R16B Rev B

MSL Table

Part Number	MSL Rating
SID1183K	3

ESD and Latch-Up Table

Test	Conditions	Results
Latch-up at 125 °C	JESD78D	> ±100 mA or > 1.5 × V_{MAX} on all pins
Human Body Model ESD	JESD22-A114F	> ±2000 V on all pins
Charged Device Model ESD	JESD22-C101	> ±500 V on all pins
Machine Model ESD	JESD22-A115C	> ±200 V on all pins

IEC 60664-1 Rating Table

Parameter	Conditions	Specifications
Basic Isolation Group	Material Group	I
Installation Classification	Rated mains voltage ≤ 150 V_{RMS}	I - IV
	Rated mains voltage ≤ 300 V_{RMS}	I - IV
	Rated mains voltage ≤ 600 V_{RMS}	I - IV
	Rated mains voltage ≤ 1000 V_{RMS}	I - III

Electrical Characteristics (EMI) Table

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Common-Mode Transient Immunity, Logic High	CM_H	Typical values measured according to Figures 33, 34. Maximum values are design values assuming trapezoid waveforms		-35 / 50	-100 / 100	kV/µs
Common-Mode Transient Immunity, Logic Low	CM_L	Typical values measured according to Figures 33, 34. Maximum values are design values assuming trapezoid waveforms		-35 / 50	-100 / 100	kV/µs
Variable Magnetic Field Immunity	H_{HPEAK}	See Note 15		1000		A/m
	H_{LPEAK}	See Note 15		1000		

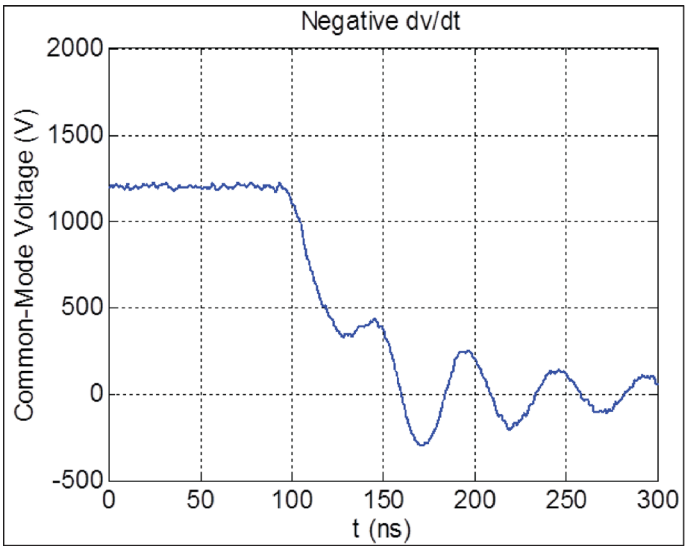


Figure 33. Applied Common Mode Pulses for Generating Negative dv/dt.

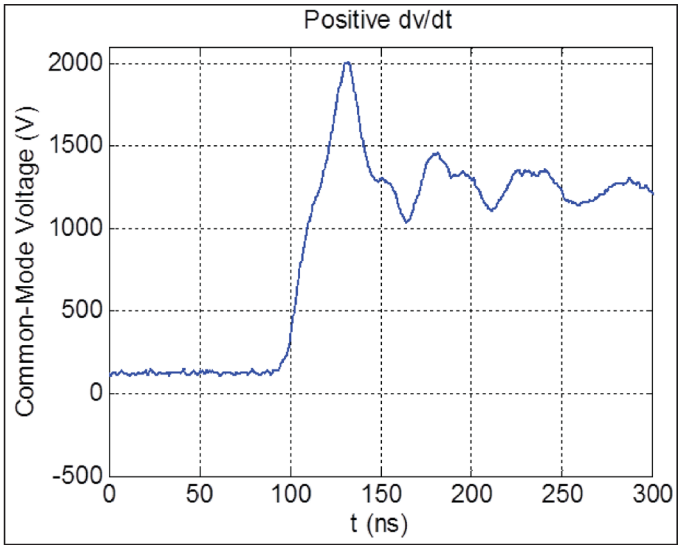


Figure 34. Applied Common Mode Pulses for Generating Positive dv/dt.

Regulatory Information Table

VDE	UL	CSA
Certified to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12	UR recognized under UL1577 Component Recognition Program	UR recognized to CSA Component Acceptance Notice 5A
Basic insulation for Max. Transient Isolation voltage 8 kV_{PEAK}, Max. Surge Isolation voltage 8 kV_{PEAK}, Max. Repetitive Peak Isolation voltage 1700 V_{PEAK}	Single protection, 5000 V_{RMS} dielectric voltage withstand	Single protection, 5000 V_{RMS} dielectric voltage withstand
File No. 5020828-4880-0002	File No. Pending	File No. Pending

Part Ordering Information

SID 1183 K - TL

- **SCALE-iDriver Product Family**
- **Series Number**
- **Package Identifier**
  - K — eSOP-R16B
- **Tape & Reel and Other Options**
  - Blank — Tube of 48 pcs.
  - TL — Tape & Reel, 1000 pcs min/mult.

Notes

Revision	Notes	Date
A	Code A Initial Release.	05/17

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