Overview

The **Vortex86EX** is a high performance and fully static 32-bit X86 processor with the compatibility of Windows based, Linux and most popular 32-bit RTOS. It also integrates 16KB write through 4-way L1 cache, 128KB write through/write back 4-way L2 cache, PCIE bus in at 2.5 GHz, DDR3, ROM controller, xISA, I2C, SPI, IPC (Internal Peripheral Controllers with DMA and interrupt timer/counter included), Fast Ethernet, FIFO UART, USB2.0 Host and SD/SATA controller within a single 288-pin LBGA package to form a system-on-a-chip **(SOC)**. It provides an ideal solution for the embedded system to bring about desired performance.

Features

- **X86 Processor Core**
  - 6-stage pipeline
- **Floating point unit support**
  - Extends CPU instruction set to include Trigonometric, Logarithmic and Exponential
  - Implements ANSI/IEEE standard 754-1985 for binary Floating-Point Architecture
- **Branch prediction unit**
  - Branch target buffer
- **Translation Lookaside buffer**
  - 32 I/D translation lookaside buffer
- **Embedded I / D Separated L1 Cache**
  - 16K I-Cache, 16K D-Cache
- **Embedded L2 Cache**
  - 4-way 128KB L2 Cache
  - Write through or write back policy
- **DDRIII Control Interface**
  - 16 bits data bus
  - 2 rank
  - DDRIII clock support up to 300MHz
  - DDRIII size support up to1Gbytes
- **SD Interface**
  - SD x 1 at IDE Primary Channel
- **SATA Interface**
  - SATA 1.5G (1 Port) at IDE Secondary Channel
- **Ethernet MAC Controller + PHY**
- **PCIE Control Interface**
  - Up to 1 sets PCIE device
- **PCIE Target Interface**
- **USB 2.0 Host Support**
  - Supports HS, FS and LS
  - 2 port
- **USB 1.1 Device Support**
  - 1 port
  - Supports FS with 3 programmable endpoint
- **HDA Controller**
  - 1 input stream, 1 output stream
- **ADC Interface x 8**
- **I^2C bus**
  - Compliant w/t V2.1
  - Some master code (general call, START and CBUS) not support.
- **SPI Boot Interface**
  - For boot up function from SPI flash
  - Half duplex
  - Support SPI Flash Size up to 128MB
- **Full Duplex SPI Controller**
  - Some master code (general call, START and CBUS) not support.
  - Support SPI Device x2 (Chip Select x2)
- **CAN Bus Controller**
- **Motor Control Interface Support**
  - 1groups of controller, 4 controllers per group
  - Each controller can configure to PWM/Servo/Sensor Interface mode
  - Controller interconnect to the other with routing network in the same group
- **xISA Bus Interface**
  - AT clock programmable
  - 8/16 Bit xISA device with Zero-Wait-State
  - Generate refresh signals to xISA interface during DRAM refresh cycle
  - Support Max xISA Clock 33M
- **DMA Controller**
- **Interrupt Controller**
- **MTBF Counter**
- **Counter / Timers**
  - 1 sets of 8254 timer controller
- **Real Time Clock**
  - Less than 2.5uA (3.0V) power consumption in Internal RTC Mode while chip is power-off.
- **FIFO UART Port x 10 (10 sets COM Port)**
  - Compatible with 16C550 / 16C552
  - Default internal pull-up
  - Supports the programmable baud rate generator with the data rate from 50 to 6M bps
  - The character options are programmable for 1 start bits; 1, 1.5 or 2 stop bits; even, odd or no parity; 5~8 data bits
  - Support TXD_En Signal on COM1-8
  - Port 80h output data could be sent to COM1 by software programming
  - Support half-duplex mode
- **Parallel Port**
  - Supports SPP/EPP/ECP mode
- **General Programmable I/O**
  - Supports 80 programmable I / O pins
  - Each GPIO pin can be individually configured to be an input/output pin
  - GPIO_P0~GPIO_P9 can be program by 8051A
  - All GPIO port with interrupt support (input/output)
- **PS / 2 Keyboard and Mouse Interface Support**
  - Compatible with 8042 controller

- **Speaker out**
- **JTAG Interface supported for S.W. debugging**
- **Input clock**
  - 25 MHz
  - 32.768 KHz
- **Output clock**
  - one clock output select from 14.318MHz /24MHz / 25MHz/ xISA Clock
- **Operating Voltage Range**
  - Core voltage: 1.2 V ± 5%
  - I / O voltage: 1.5V ± 5% , 3.3 V ± 10 %
- **Operating temperature**
  - -40℃ ~ 85℃
- **Package Type**
  - 16x16mm TFBGA-288

Block Diagram